LZ2414J

1/4 type B/W CCD Area Sensor for EIA

DESCRIPTION

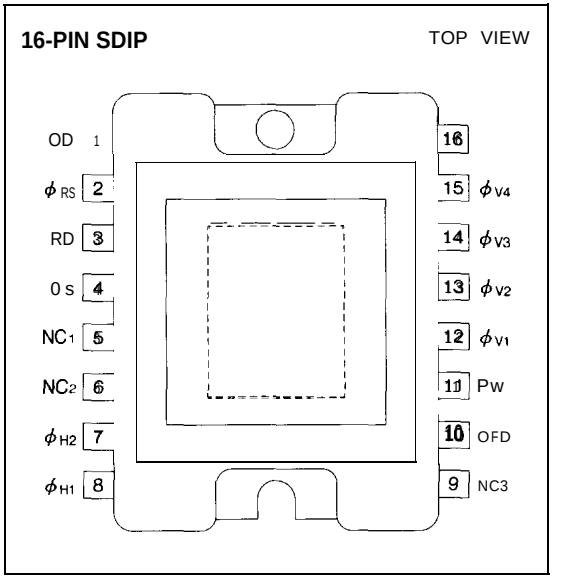
LZ2414J is a 1/4-type (4.5 mm) solid-state image sensor that consists of PN phote-diodes and CCDS (charge-coupled devices). Having approximately 270000 pixels (horizontal 542 X vertical 492), the sensor provides a high resolution stable B/W image.

FEATURES

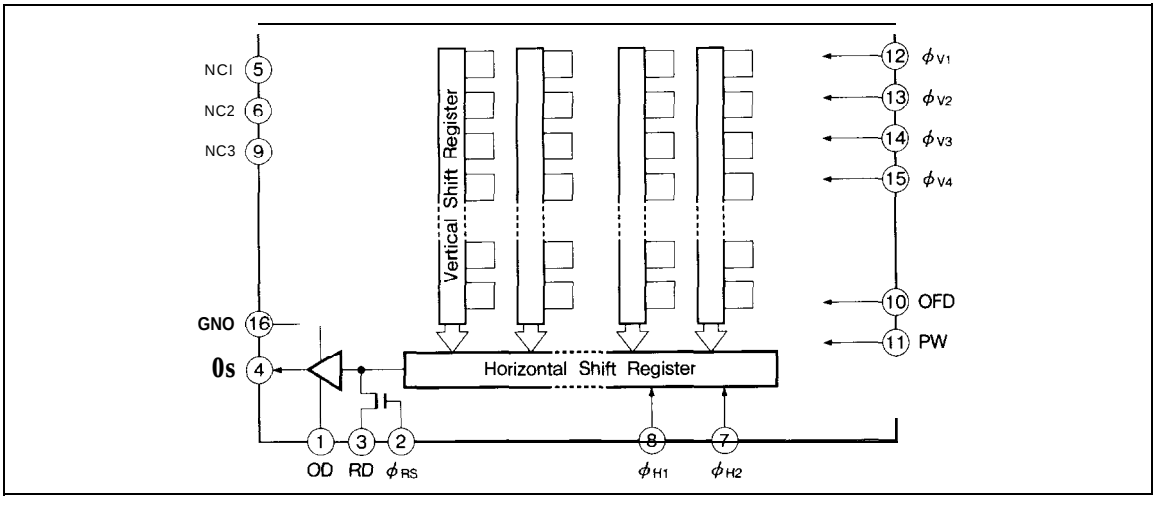
- Number of pixels : 512 (H) X 492 (V)
  Pixel pitch : 7.2 μm (H) × 5.6 μm (V)
  Number of optical black pixels
  : Horizontal; front 2 and rear 28
- Low fixed pattern noise and lag
- No burn-in and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/60 to 1/10 000 s)
- Compatible with EIA standard
- Package : 16-pin SDIP [CERDIP] (WDIP016-N-0500B)

PIN CONNECTIONS

16-PIN SDIP TOP VIEW



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
RD	Reset transistor drain
OD	Output transistor drain
0S	Video output
ϕ_{RS}	Reset transistor clock
$\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$	Vertical shift register clock
ϕ_{H1}, ϕ_{H2}	Horizontal shift register clock
OFD	Overflow drain
PW	P lype well
GND	Ground
NC1 , NC2, NC3	No connection

ABSOLUTE MAXIMUM RATINGS

(Ta = 25-C.)

PARAMETER	SYMBOL	RATING	UNIT
Output transistor drain voltage	V_{OD}	Oto +18	V
Reset drain voltage	V_{RD}	Oto +18	V
Overflow drain voltage	V_{OFD}	o to +55	V
Reset gate clock voltage	$V_{\phi RS}$	–0,3 to +18	V
Vertical shift register clock voltage	$V_{\phi V}$	–9.0 to +18	V
Horizontal shift register clock voltage	$V_{\phi H}$	–0.3 to +18	V
Voltage difference between PW and vertical clink	$V_{PW} - V_{\phi V}$	–28 to O	V
Storage temperature	Tstg	–20 to +80	℃
Operating ambient temperature	Topr	–20 to +70	℃

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Operating ambient temperature		Topr		25.0		℃	
Output transistor drain voltage		VOD	14.5	15.0	16.0	v	
Reset transistor drain voltage		VRD		Voo		v	
Overflow drain voltage	When DC is applied	VOFD	5.0		19,0	v	1
	When pulse is applied p-p level	Vφ OFD	23.0			v	2
Ground		GND		0.0		v	
P-well voltage		VPW	– 10.0		V4VL	V	
Vertical shift register clock	LOW level	Vφ V1L, Vφ V3L Vφ V2L, Vφ V4L	– 8.5	– 8.0	– 7.5	V	
	INTERMEDIATE level	Vφ V1I, Vφ V3I Vφ V2I, v φ V4I		0.0		V	
	HIGH level	Vφ V1H, Vφ V3H	17.0	17.5	18.0	v	
Horizontal shift resistor clock	LOW level	Vφ H1L, Vφ H2L	– 0.05	0.0	0.05	v	
	HIGH level	Vφ H1H, Vφ H2H	4.7	5.0	6.0	v	
Reset gate clock	LOW level	Vφ RSL	0.0		Voi)–13.0	v	
	HIGH level	Vφ RSH	VOD – 8.5		10.0	v	
Vertical shift register clock frequency		fφ V1, fφ V2 fφ V3, fφ V4		15.73		kHz	
Horizontal shift register clock frequency		fφ H1, fφ H2		9.53		MHz	
Reset gate clock frequency		fφ RS		9.53		MHz	

* Connect NC1, NC2 and NC3 to GND directly or through a capacitor lager than 0.047 μF

NOTES :

1. When DC voltage is applied, shutter speed is 1/W seconds.
2. When pulse is applied, shutter speed is less than 1/~ seconds.

ELECTRICAL CHARACTERISTICS (Drive method : Field Accumulation)

(Ta= 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Standard output voltage	Vo		150		mV	2
Photo response non-uniformity	PRNU			15	0/0	3, 4
Saturation output voltage	Vsat	700			mV	3, 5
Dark output voltage	Vdark		0.5	3.0	mV	1, 6
Dark signal non-uniformity	DSNU		0.5	2.0	mV	1, 3, 7
Sensitivity	R	250	350		mV	8
Smear ratio	SMR		– 80	– 72	dB	9, 10
Image lag	AI			1.0	%	11
Blooming suppression ratio	ABL	1000				9, 12
Output transistor drain current	I_{OD}		4,0	8.0	mA	
Output impedance	R_O		350		Ω	

NOTES :

1 Ta : +60°C

2 The average output voltage under the uniform i Illumination. The standard exposure condition is defined when Vo is 150 mV.

3 The image area is divided into 10x 10 segments. The sagment's voltage is the average output voltage of all the pixels within the segment.

4 PRNU is defined by (Vmax – Vmin)/Vo, where Vmax and Vmin are the maximum and the minimum values of each segment's voltage respectively, under the standard exposure condition.

5 The minimum segment's voltage under 10 times exposure of the standard exposure condition.

6 The average output voltage under the non-exposure condition.

7 DSNU is defined by (Vdmax – Vdmin), where Vdmax and Vdmin are the maximum and the minimum values of each segment's voltage respectively, under the non-exposure condition.

8 The average output voltage when a 1 000 lux light source with a 90% reflector is imaged with a lens at F4, f50 mm.

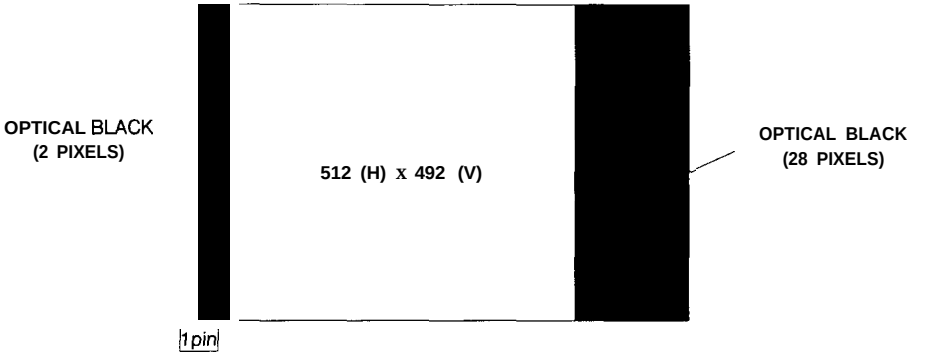
9 The sensor is exposed only in the central area of V/l O square, where V is the vertical image size.

10 SMR is defined by the ratio of the smear voltage detected during the vertical blanking period to the maximum output voltage in the V/10 square, with a lens at F4.

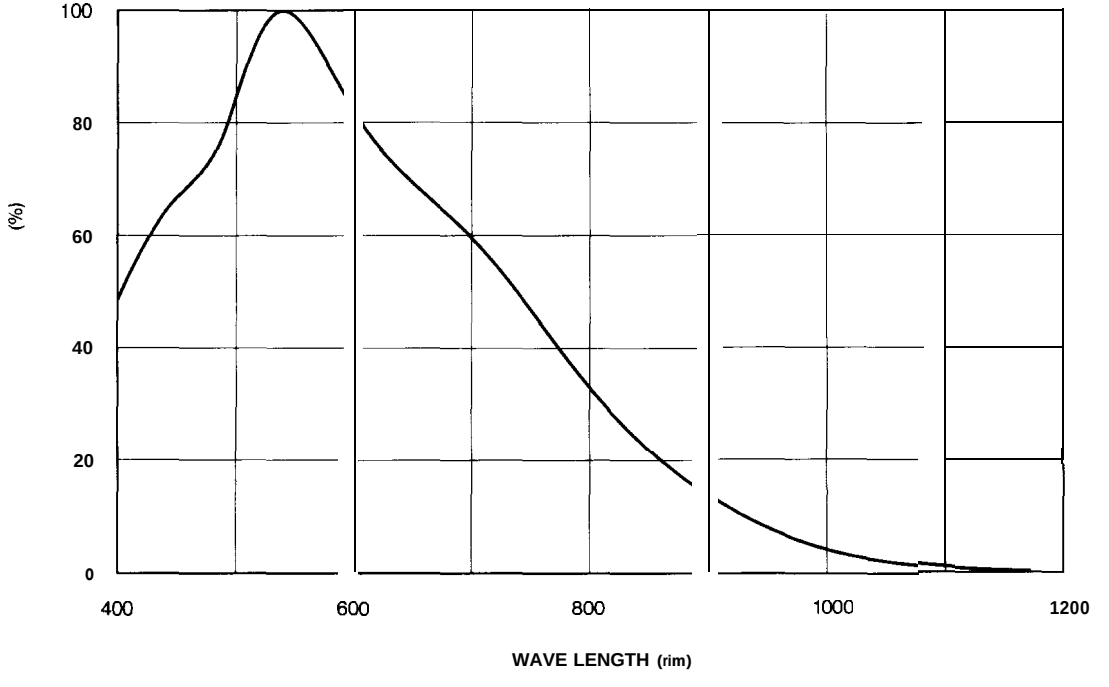
11 The sensor is exposed at the exposure level corresponding to the standard condition. AI is defined by the ratio of the lag voltage measured at the 1st field during the non-exposure period to the standard output voltage.

12 ABL is defined by the ratio of the exposure at the standard condition to the exposure at a point where a blooming is observed.

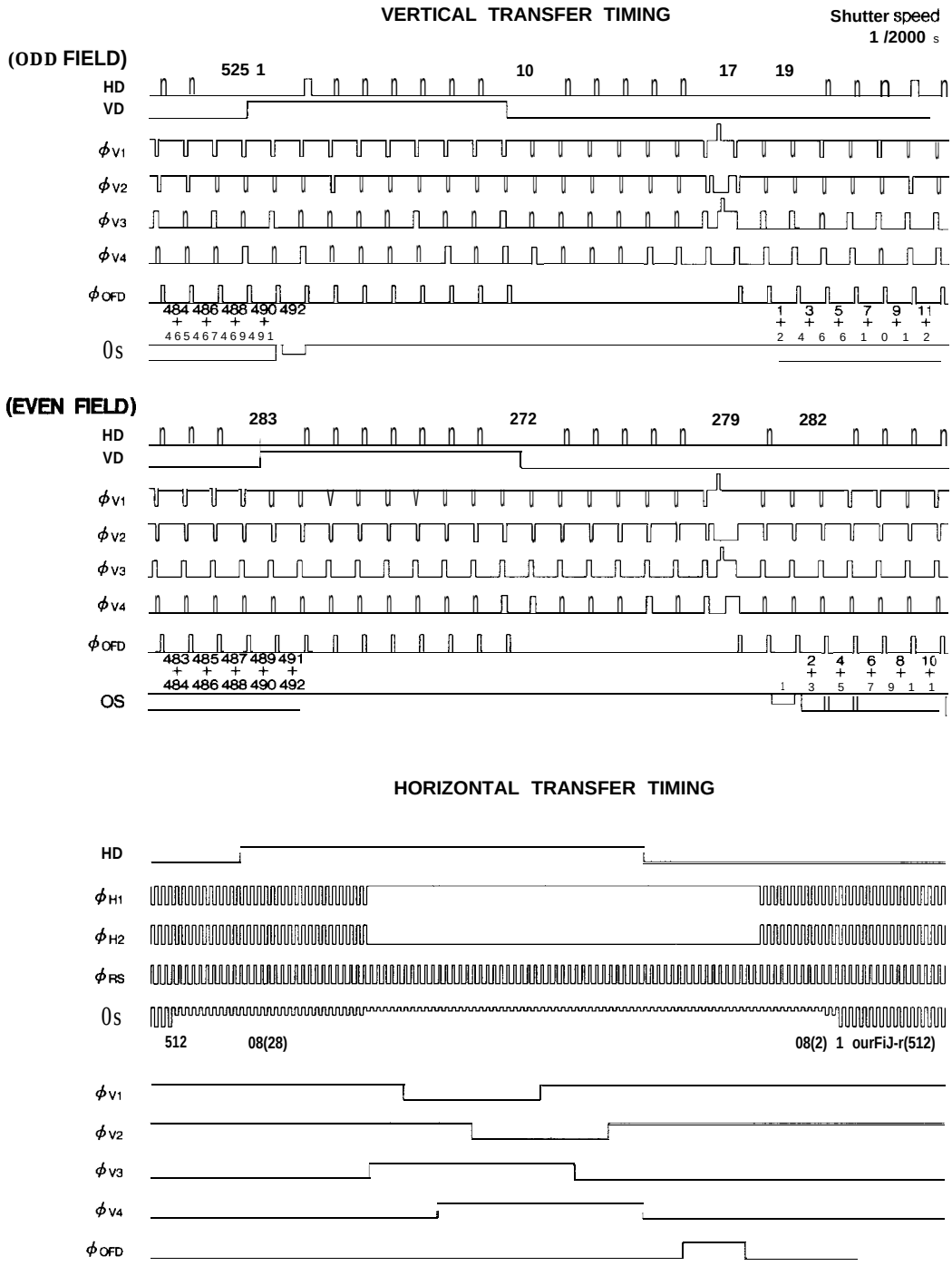
PIXEL STRUCTURE



SPECTRAL RESPONSE EXAMPLE

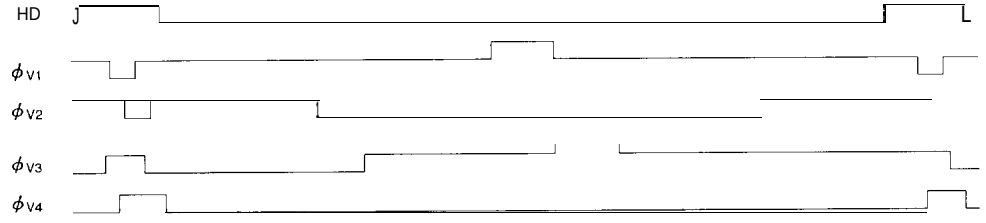


TIMING DIAGRAM EXAMPLE

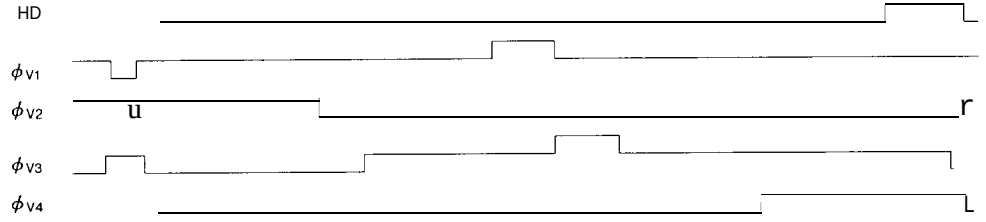


READOUT TIMING

(ODD FIELD)



(EVEN FIELD)



SYSTEM CONFIGURATION EXAMPLE